[EUREC-725A]
B.Tech. DEGREE EXAMINATION
Electronics & Communication Engineering
VII SEMESTER
DIGITAL DESIGN THROUGH VERILOG
(Effective from the admitted batch 2012–13)

Time: 3 Hours
Max.Marks: 60

Instructions: Each Unit carries 12 marks.
Answer all units choosing one question from each unit.
All parts of the unit must be answered in one place only.
Figures in the right hand margin indicate marks allotted.

UNIT-I
1. a) Describe in detail about the system tasks 6
   b) Differentiate between synthesis and simulation 6
   OR
2. a) What are the different levels of design description? Explain briefly 6
   b) Explain the problems experienced at the time of debugging 6

UNIT-II
3. a) Explain continuous assignments and strengths with example 6
   b) Explain delays with continuous assignments 6
   OR
4. Write a short note on:
   a) Tristate gates and delays 6
   b) Initial construct and always construct 6

UNIT-III
5. a) Design a half adder module with time delay assignment through parameter declaration 6
   b) Write test bench, simulation results for the above 6
   OR
6. a) Write a verilog code for D flip flop using NAND gates 6
   b) Explain continuous assignment structures with examples 6

UNIT-IV
7. a) Define a state machine chart. Describe a FSM for Moore machine with one test per one state 6
   b) Write a note on the linked state machine in detail 6
   OR
8. a) Implement a dice game using microprogramming 6
   b) Realize a state machine chart for mealay machine 6

UNIT-V
9. With the help of a neat sketch describe the SRAM memory interfacing process to the microprocessor bus 12
   OR
10. Design and verify the HDL module for UART receiver 12