Integrated Dual Degree (B.Tech.+M.Tech.) Examination
Electronics & Communication Engineering
VII SEMESTER
ANALOG IC DESIGN
(Effective from the admitted batch 2010–11)

Time: 3 Hours  Max.Marks: 60

Instructions: Each Unit carries 12 marks.
Answer all units choosing one question from each unit.
All parts of the unit must be answered in one place only.
Figures in the right hand margin indicate marks allotted.

UNIT-I
1. a) Explain (i) Body Effect (ii) Channel Length Modulation
b) For figure given below plot transconductance as function of $V_{DS}$

![MOS Device Diagram]

OR

2. Discuss in detail about the MOS Device models

UNIT-II
3. a) Explain the operation of folded cascade
b) Explain the operation of common gate stage with (i) Direct coupling input (ii) Capacitor coupling input

OR

4. Explain in detail about the operation of Source Follower

UNIT-III
5. a) Derive small signal gain for differential pair with
   i) Diode connected load ii) Current source load
b) Explain the quantitative analysis of basic differential pair

OR

6. a) Explain the operation of basic current mirror
b) Discuss the common mode properties of differential pair with active current mirror

UNIT-IV

7. a) Explain the operation of high frequency model of a common source gate
b) Calculate transfer function of circuit given below

8. a) Explain the operation of Voltage-Voltage feedback topology
b) Calculate voltage gain of circuit given below

UNIT-V

9. a) Write short notes on (i) Power supply Rejection (ii) Slew rate in op-amps
b) Write briefly about frequency compensation of Op-Amps

OR

10. a) Write short notes on (i) Multipole systems (ii) Phase margin
b) Explain the compensation of two stage op-amp using common gate stage