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UNIT-IV

7. a) Draw the logic gate diagram and layout for the following function: 
   \[ F = xy + y'z \]  
b) Design comparator and draw its layout

OR

8. a) Design a decade counter and draw its layout  
b) Design a two bit full adder and draw its layout

UNIT-V

9. a) What is CPLD? How it is useful in VLSI design?  
b) Name some design verification tools and how these are used to design VLSI circuits

OR

10. a) Why testing is needed? Explain the chip level testing  
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